

FIG. 1A

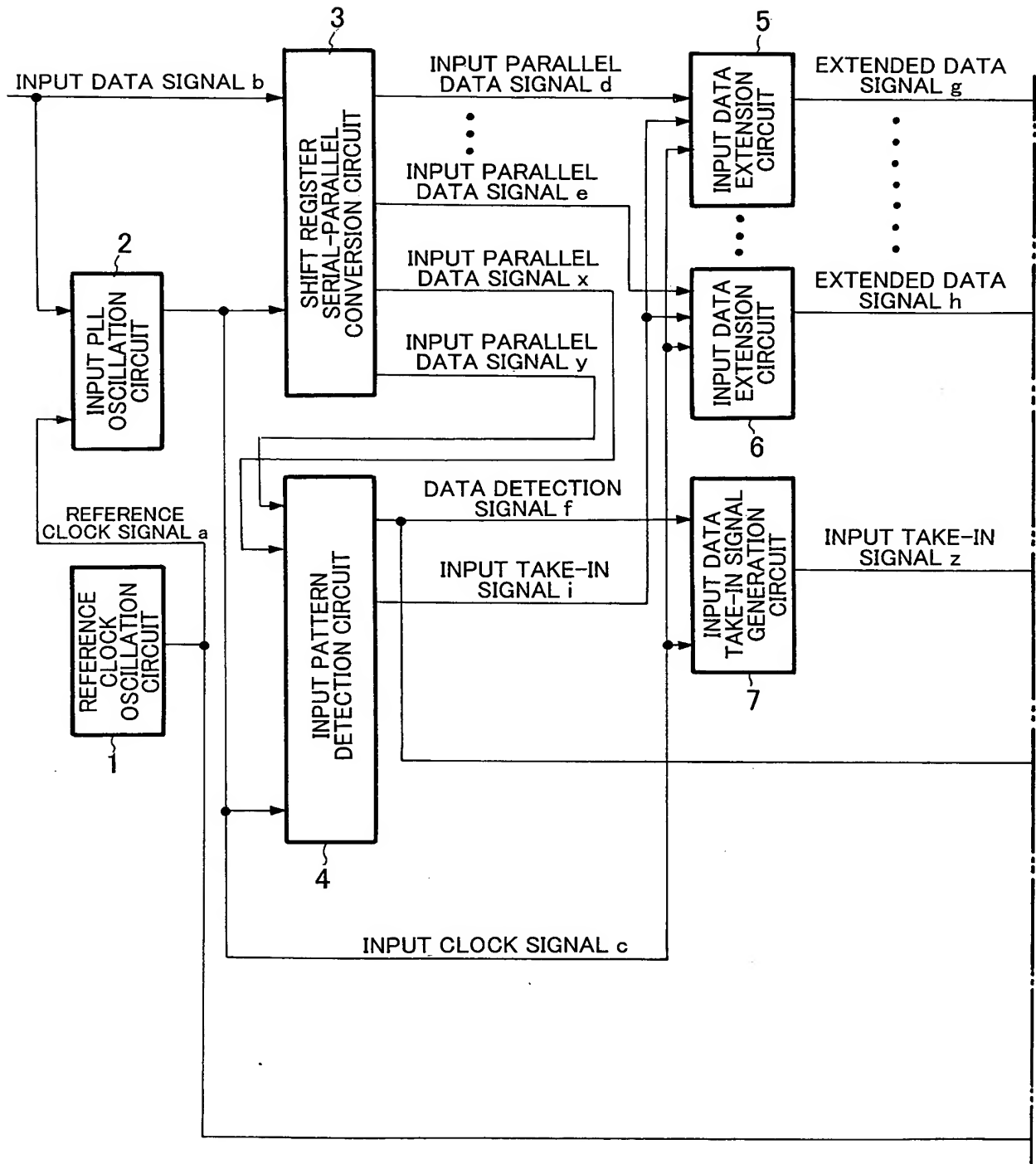


FIG. 1B

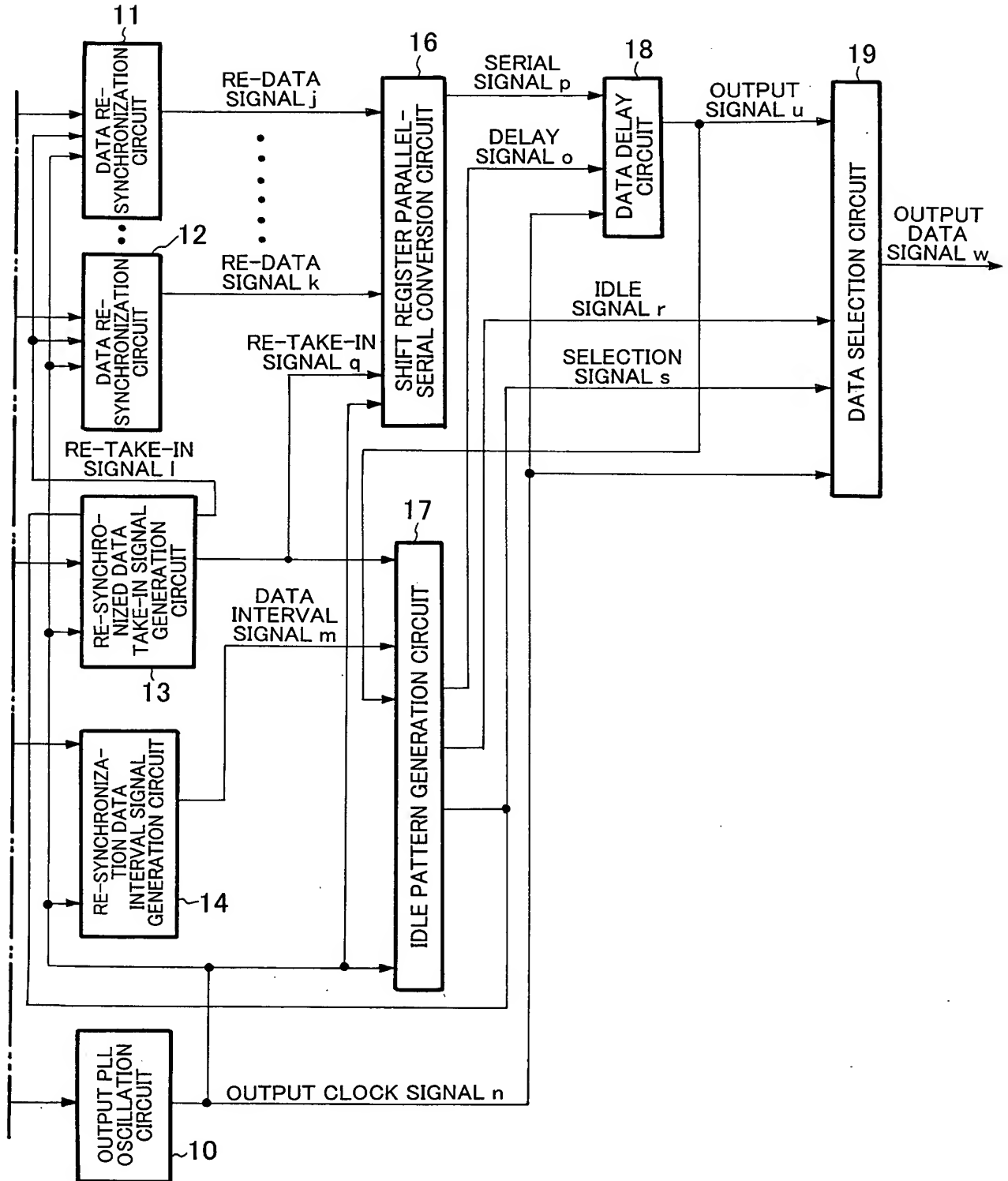


FIG.2A

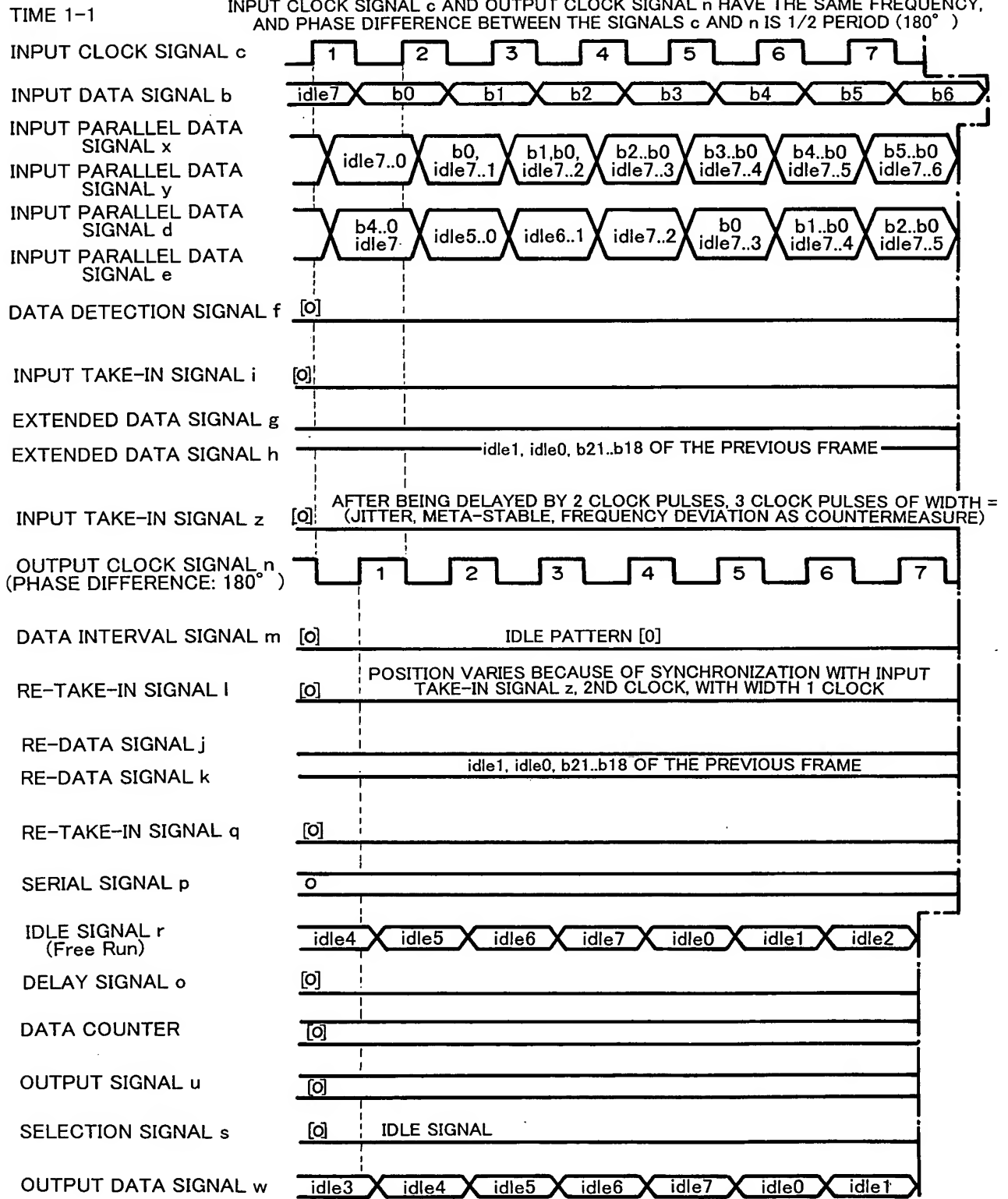


FIG.2B

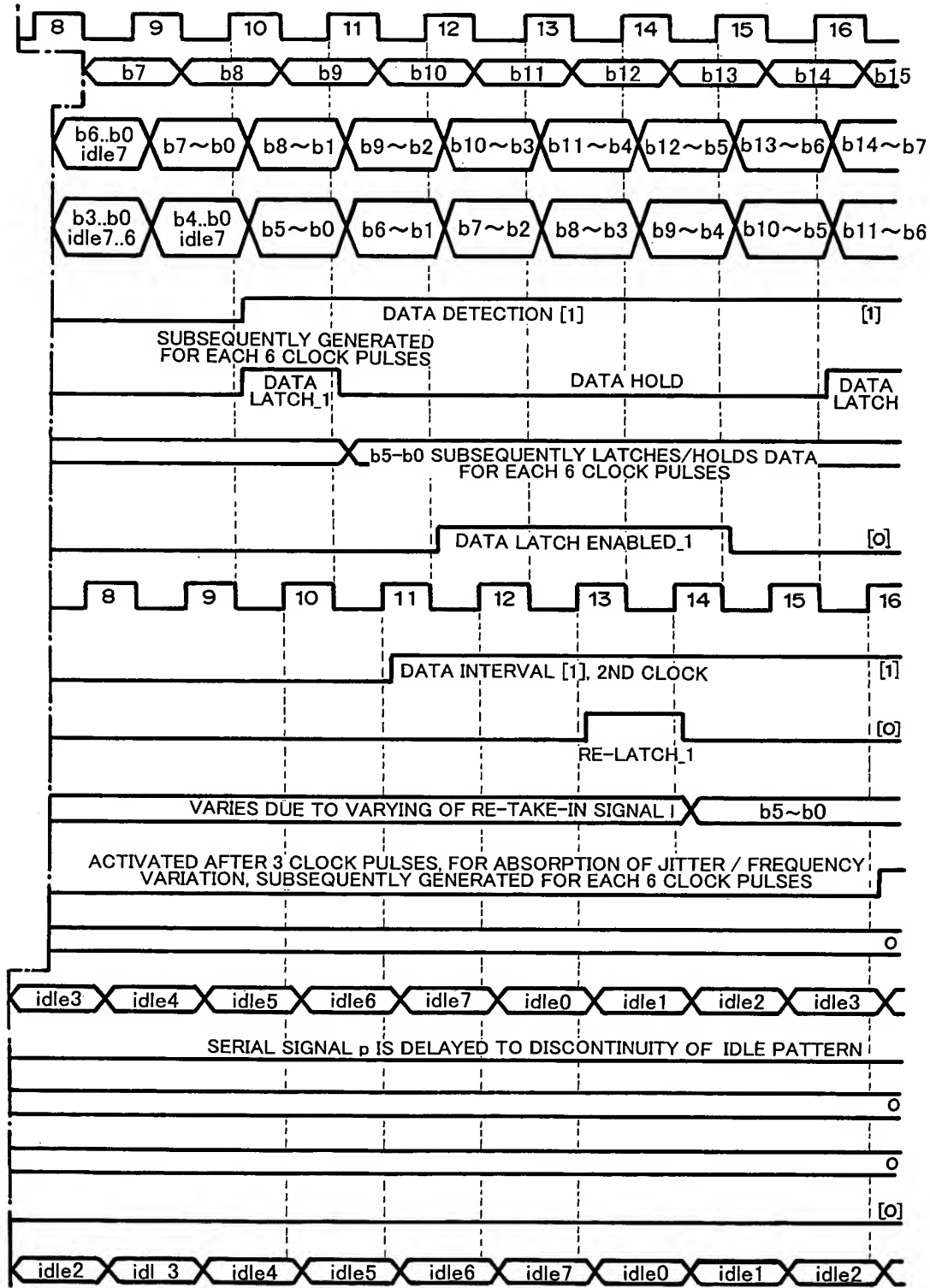


FIG.3A

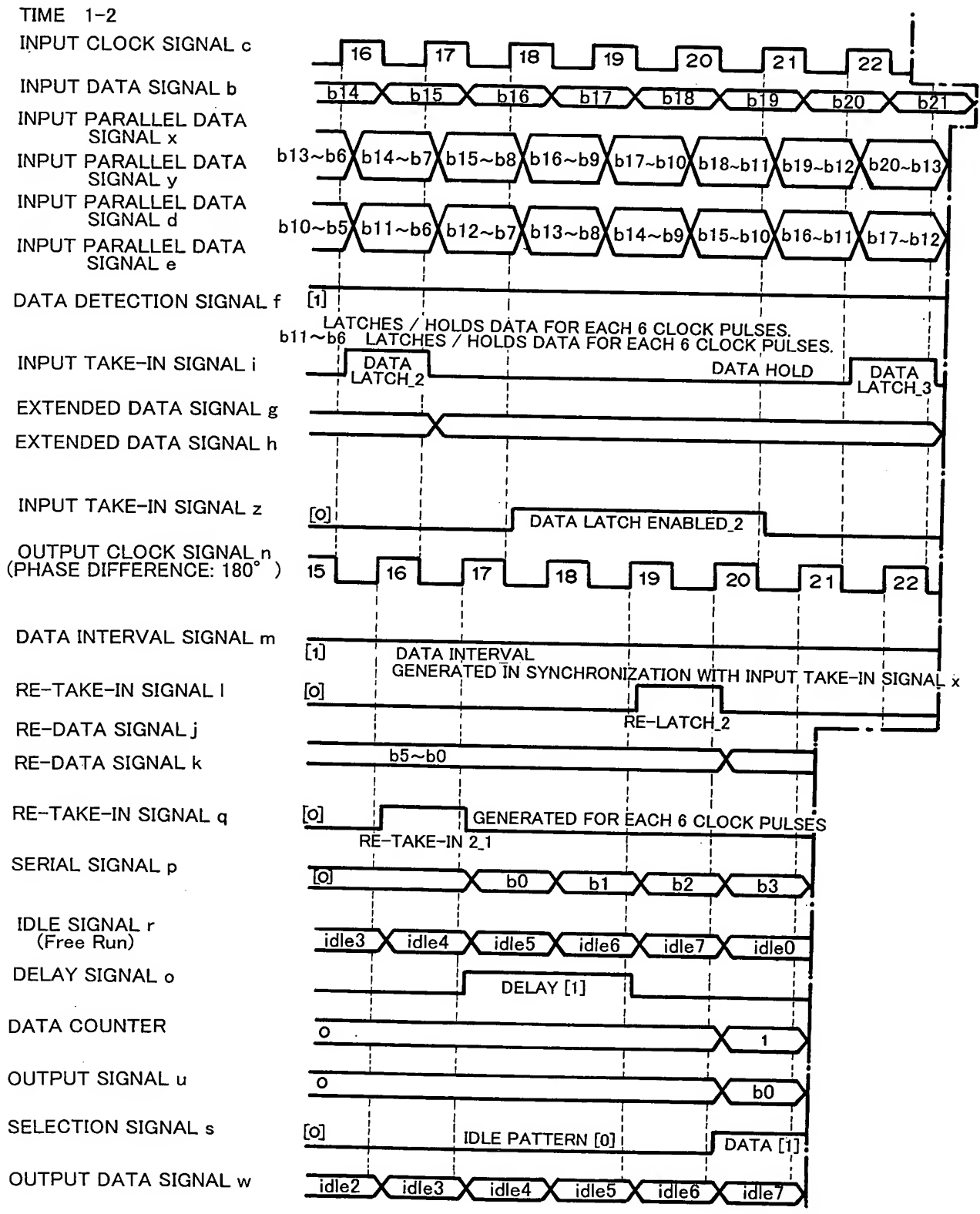


FIG.3B

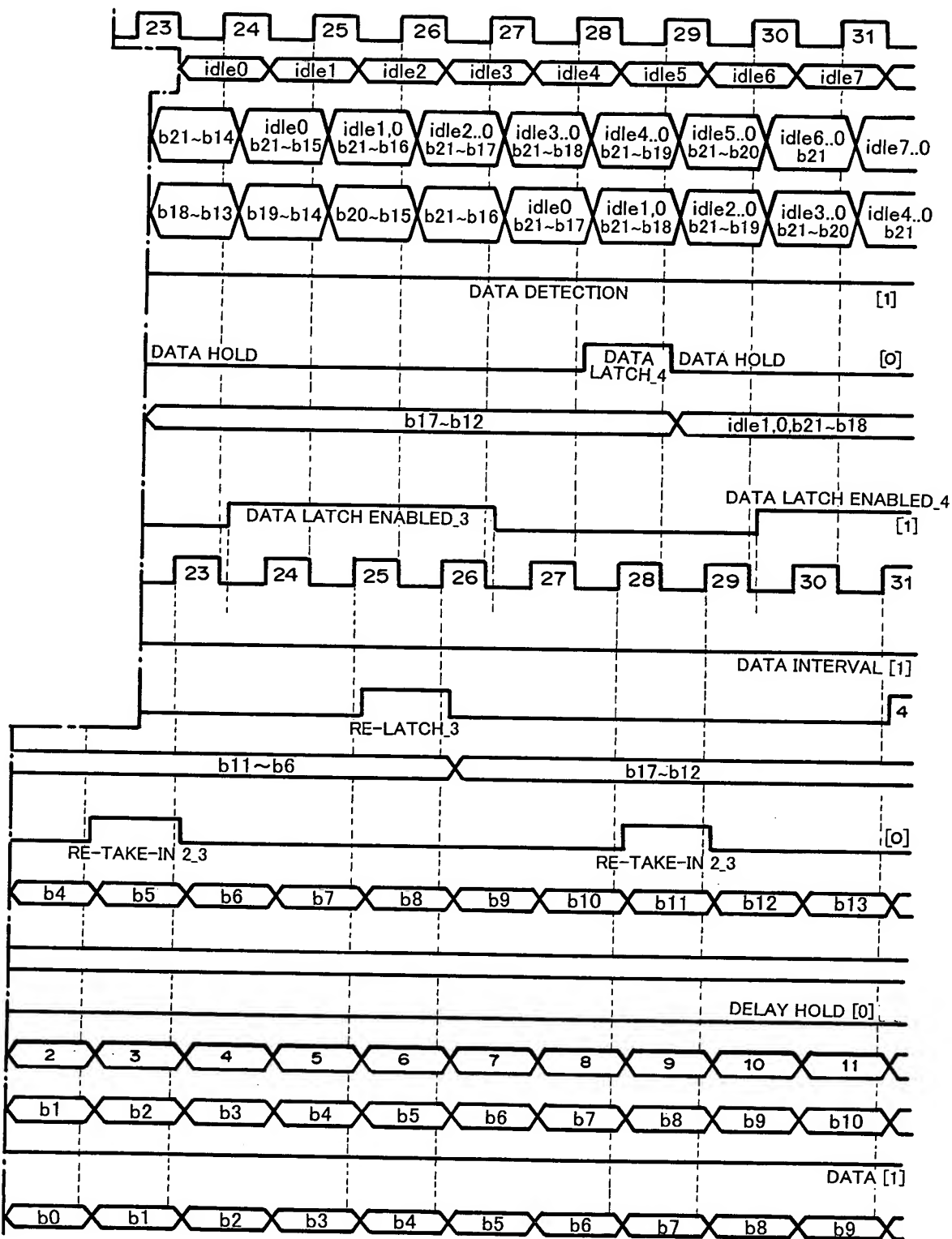


FIG.4A

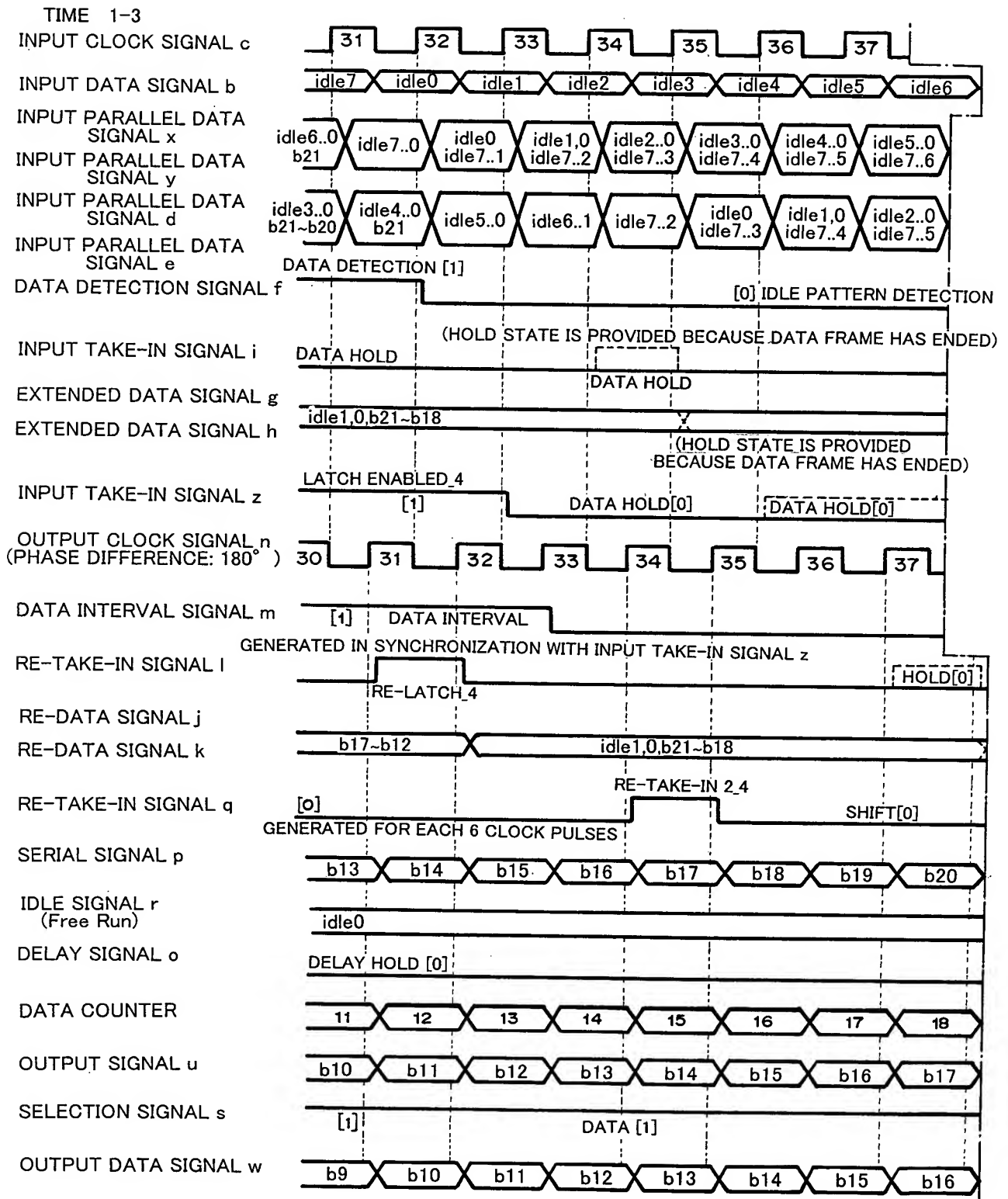


FIG. 4B

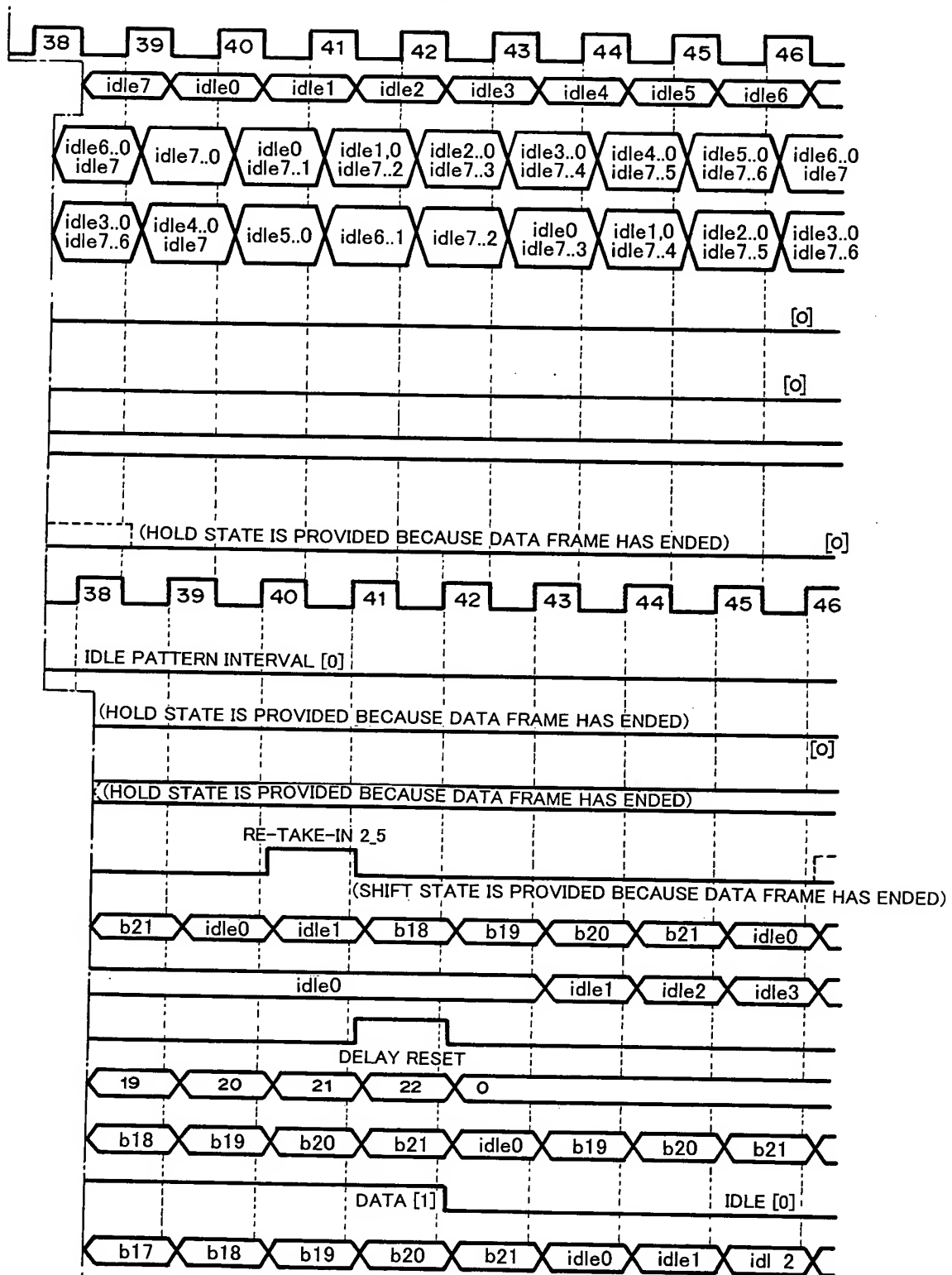


FIG.5A

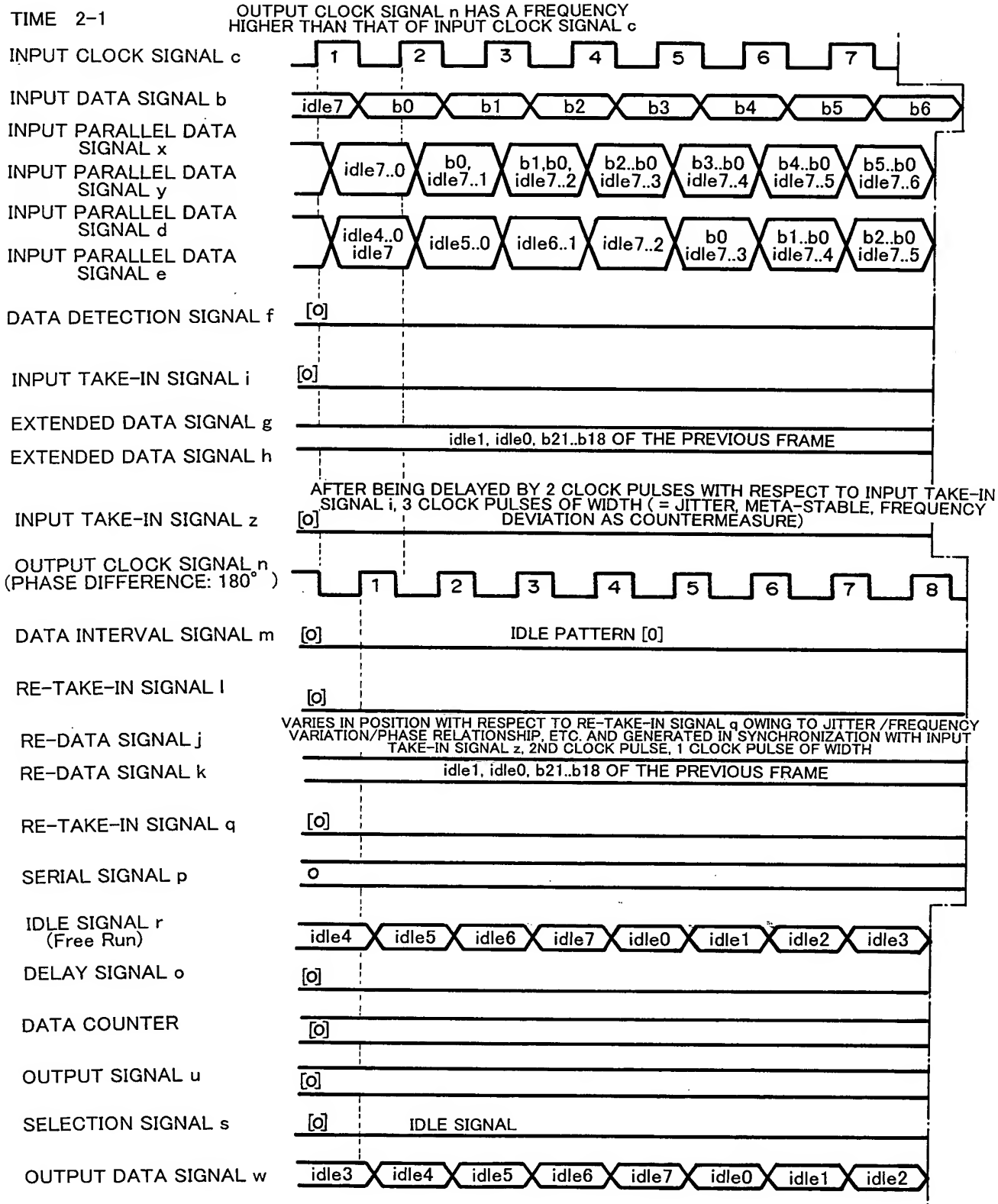


FIG.5B

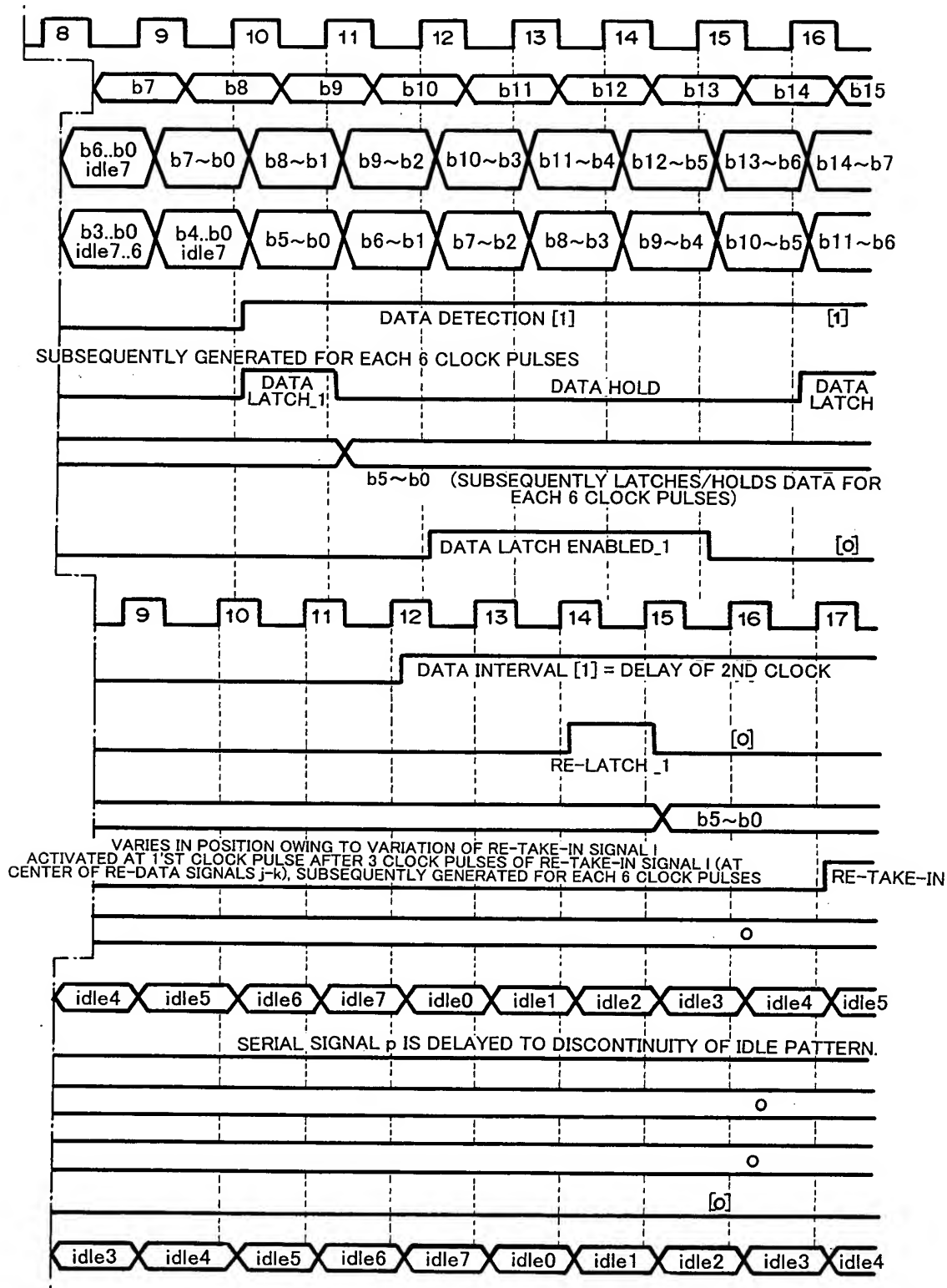


FIG.6A

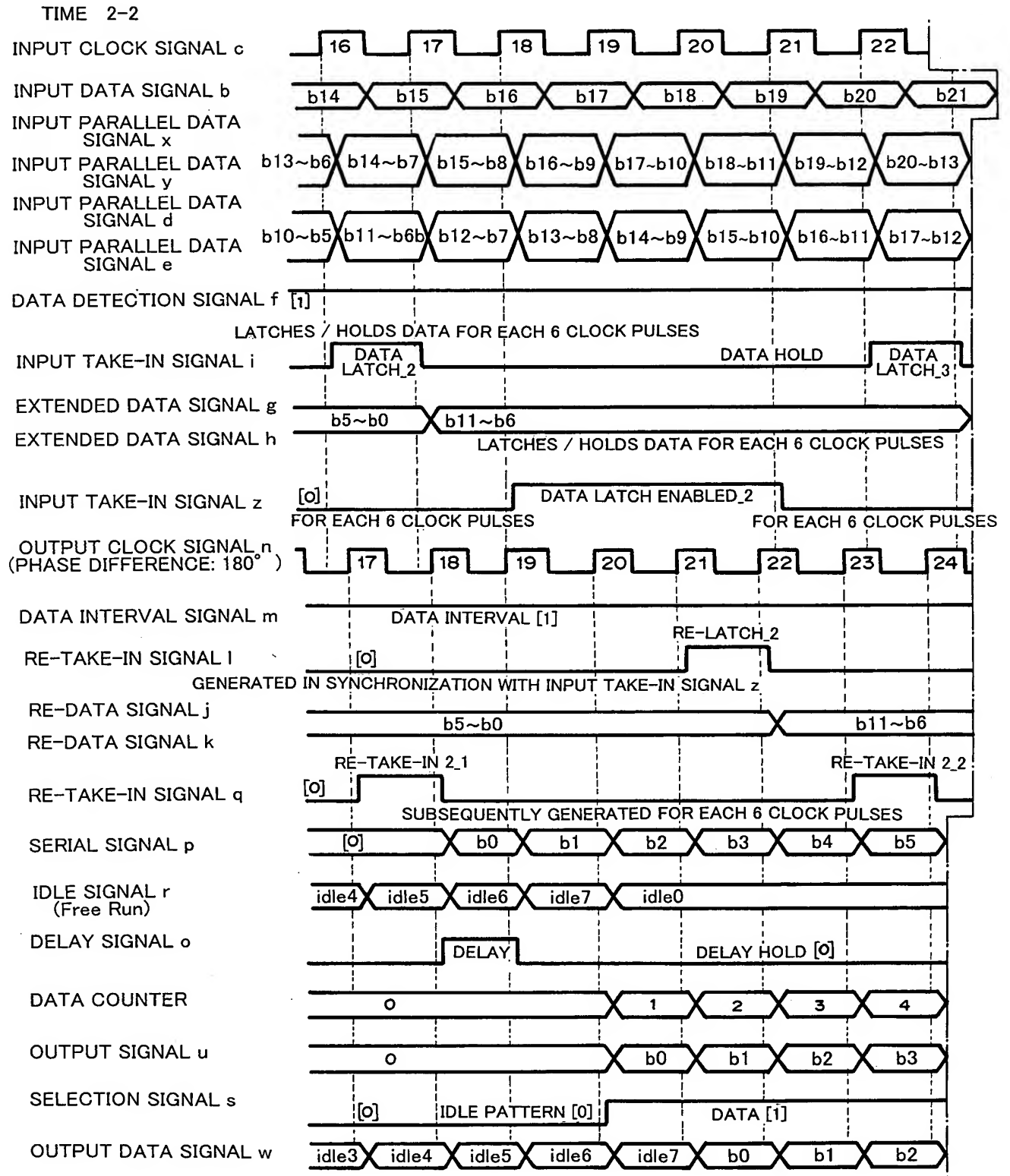


FIG. 6B

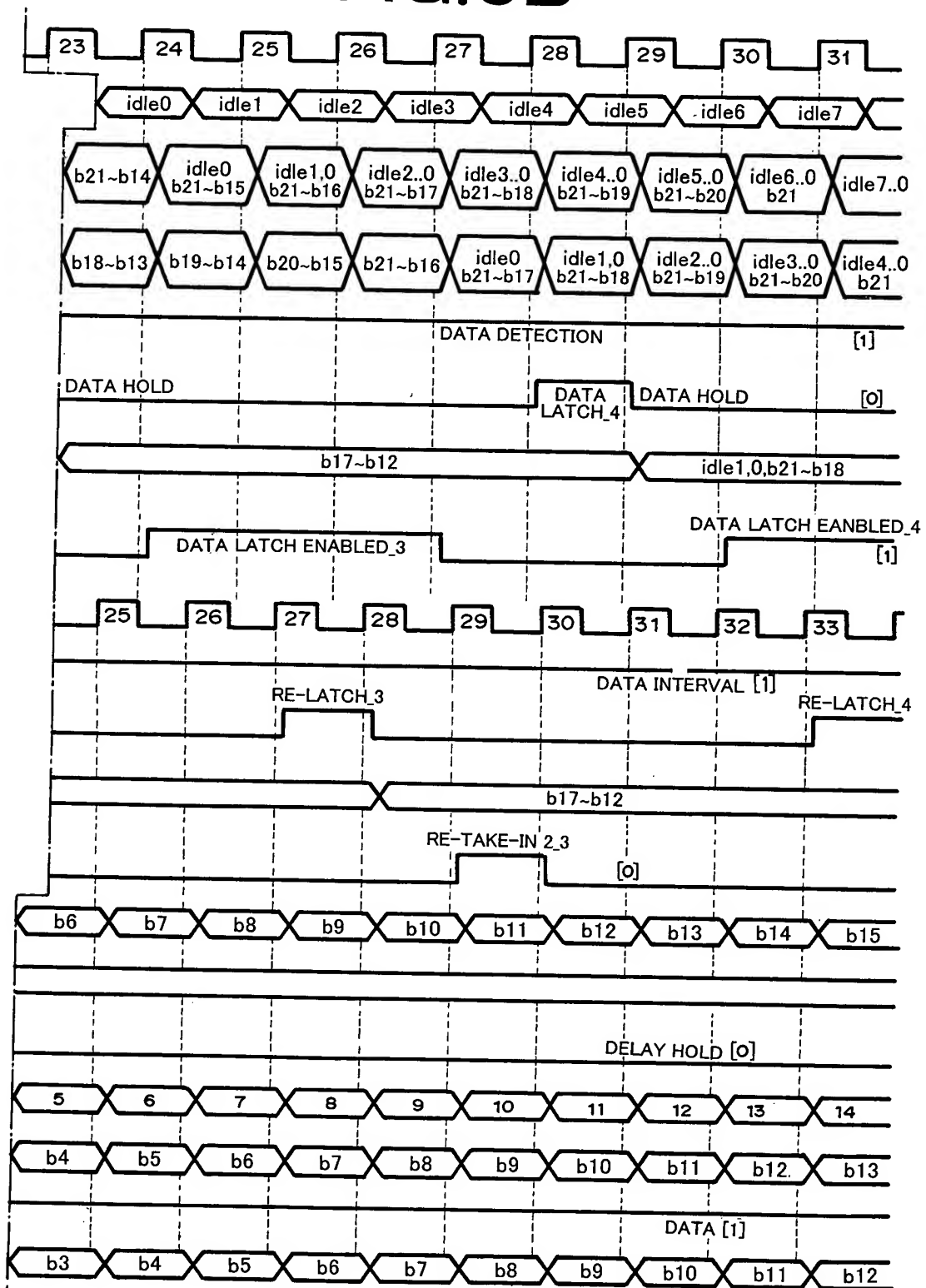


FIG.7A

TIME 2-3

INPUT CLOCK SIGNAL c

INPUT DATA SIGNAL b

INPUT PARALLEL DATA SIGNAL x

INPUT PARALLEL DATA SIGNAL y

INPUT PARALLEL DATA SIGNAL d

INPUT PARALLEL DATA SIGNAL e

DATA DETECTION SIGNAL f

INPUT TAKE-IN SIGNAL i

EXTENDED DATA SIGNAL g

EXTENDED DATA SIGNAL h

INPUT TAKE-IN SIGNAL z

OUTPUT CLOCK SIGNAL n
(PHASE DIFFERENCE: 180°)

DATA INTERVAL SIGNAL m

RE-TAKE-IN SIGNAL l

RE-DATA SIGNAL j

RE-DATA SIGNAL k

RE-TAKE-IN SIGNAL q

SERIAL SIGNAL p

IDLE SIGNAL r
(Free Run)

DELAY SIGNAL o

DATA COUNTER

OUTPUT SIGNAL u

SELECTION SIGNAL s

OUTPUT DATA SIGNAL w

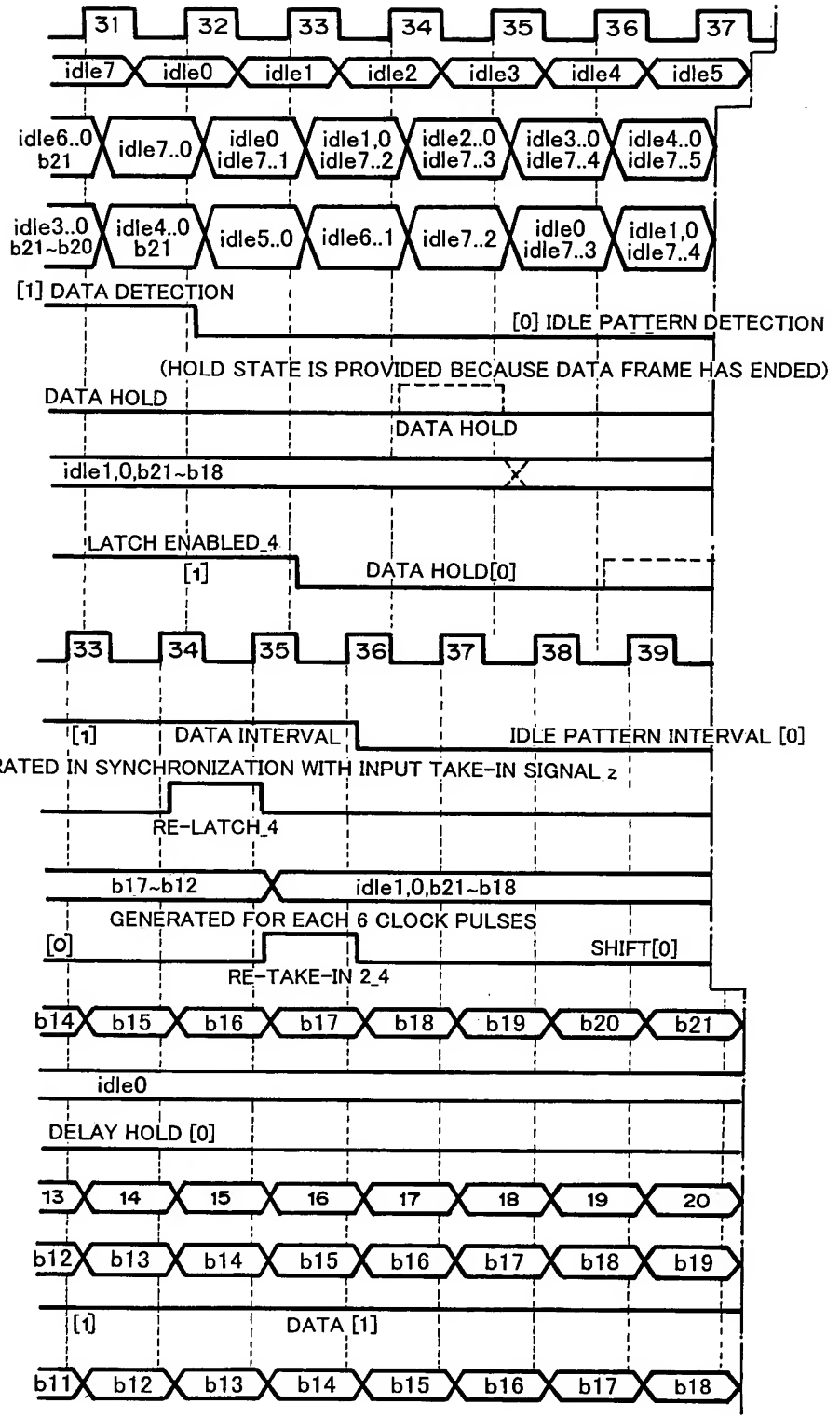


FIG. 7B

